REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1-38, as amended, will remain in the application.

Specification

The specification has been amended to correct informalities.

Claim Objections

The claims have been amended to correct informalities.

Claim Rejections – 35 USC § 102

Claims 1-24 and 26-38 were rejected under 35 U.S.C. 102(b) as being allegedly anticipated by Crouch et al. (U.S. Patent No. 5,995,731, hereinafter "Crouch").

Applicant teaches a tiered memory testing architecture including a first tier in which a single, centralized BIST controller is used to control memory tests on multiple memories by issuing generalized commands to sequencers at a second tier, each sequencer associated with memory modules sharing a common clock domain. At the third tier, memory interfaces, each associated with a corresponding memory module, handle specific interface requirements for each memory module, e.g., based on the specific timing requirements and physical characteristics of the memory modules. Advantages of this hierarchical BIST architecture is that area is conserved and overhead for the BIST controller only happens once, whether for testing a couple of memory modules or dozens.

Crouch describes a typical memory testing architecture in which a BIST controller is proved for each memory module. This approach is expensive in terms of area and overhead for the BIST controllers during testing. The Action cites col. 7, l. 56 to col. 8, l. 3 which describes a "combination parallel-sequential" operation. However, this refers to an architecture in which a BIST controller is provided for each memory module, and refers to staging BIST modules in a combination parallel-sequential manner.

Each of independent claims 1, 26, and 28 recite a single, centralized BIST controller for issuing commands for testing multiple memory modules. Crouch does not describe such a system, but rather a typical BIST architecture in which a BIST controller is provided for each memory module. Accordingly, Applicant submits that these claims and their dependencies are allowable.

Claim Rejections – 35 USC § 103

Claims 1-10, 12, 25 and 28 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Ledford et al. (U.S. Patent No. 6,347,056, hereinafter "Ledford").
Ledford teaches a system including a BIST controller (10) with one sequencer (16) that provides test algorithm information to multiple memories.

Applicant teaches that the sequencers and memory modules may be organized in a hierarchy, with each sequencer being associated with memory module(s) operating on a common clock domain (page 6, lines 7-12). In this manner, logic for controlling application timing and sequencing of the test pattern for the memory modules operating on a common clock domain may be incorporated within a common sequencer. The claims have been amended to recite that the sequencers are associated with memory modules operating on a common clock domain and at least two of the sequencers are associated with different clock domains.

Ledford specifically describes the use of one sequencer ("In operation, Joint Interface 12 functions as an interface jointly for all of the Memory Interfaces with a single Sequencer." col. 7, lines 1-3). This eliminates the additional circuitry and chip area needed to accommodate multiple sequencers. Ledford does not teach or suggest adding sequencers to account for memory modules operating on different clock domains. Accordingly, Applicant submits independent claims 1 and 28, as amended, and their dependencies are allowable.

CONCLUSION

In light of the arguments presented above, the Applicants respectfully submit that the instant claims are patentable. Accordingly, reconsideration and allowance of this Application is earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below. Please charge any fees which may be due to Deposit Account No. 17-0026.

Respectfully submitted,

Dated: July 5, 2006 By: _____

Kenyon S. Jenckes
Reg. No. 41,873
Attorney for the Applicant

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, California 92121
Telephone: (858) 651-5363
Facsimile: (858) 658-2502